

Requirements for Ethernet Switch Semiconductors

OPEN Alliance Specification



Author & Company	OPEN Alliance
Title	Requirements for Ethernet Switch Semiconductors
Version	1.0
Date	September 28, 2016
Status	Released
Restriction Level	Public

This document specifies requirements towards Ethernet Switch Semiconductors. These requirements cover the following areas: general function, address resolution, virtual LANs, Quality of Service, filtering, diagnostics, interfacing, configuration, and time synchronization.

Version Control of Document

Version	Editor	Description	Date
1.0	Dr. Lars Völker	First release of the document.	09/28/2016

Restriction level history of Document

Version	Restriction Level	Description	Date
1.0	Public	First release of the document.	09/28/2016

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2 Introduction

This document presents requirements for Automotive Ethernet Switch Semiconductors to define a minimum requirement set for such devices. This should give guidance to semiconductor vendors on designing suitable devices. This document does not aim to replace existing standard documents like the IEEE 802.1D Standard [1]. It rather focuses on which features of existing standards are required and in what quantity.

This document covers requirements of different categories of requirements of Automotive Ethernet Switches:

- General Requirements (see section 3.1)
- Address Resolution (see section 0)
- Virtual LANs (see section 3.3)
- Quality of Service and Audio/Video Bridging (see section 3.4)
- Time Synchronization (see section 3.5)
- Filtering of Incoming Frames (see section 0)
- Diagnostics (see section 0)
- Interfaces (see section 3.8)
- Configuration (see section 0)

The requirements of this document were defined in a way that test cases for compliance testing of Automotive Ethernet Switch Semiconductors can be defined. The test cases for this are defined in another document.

3 Requirements

3.1 General Requirements (GEN)

This section describes general requirements concerning Automotive Ethernet Switches.

Requirement GEN-001:

The Ethernet Switch shall implement all "5.1 Required Capabilities" except "f) RSTP" and "g) BPDUs" of the IEEE 802.1D Standard [1].

Requirement GEN-002:

The Ethernet Switch shall implement the optional capability "c) Multiple Traffic Classes" of the IEEE 802.1D Standard [1].

Requirement GEN-003:

The Ethernet Switch shall use a non-blocking architecture.

Requirement GEN-004:

The overall bandwidth of the Ethernet Switch fabric has to be higher than the sum of bandwidth of all ingress ports.

Requirement GEN-005:

The Ethernet Switch shall operate as store and forward switch.

Requirement GEN-006:

The boot time of the Ethernet Switch with internal PHYs and up to 16 ports total (including configuration via the host processor and startup time of internal PHYs) from voltage reaches valid range until it is fully operational shall be less than **140** ms. See Section 4.1 for typical configuration REF-CONF-A.

Requirement GEN-007:

The boot time of the Ethernet Switch without internal PHYs and up to 16 ports total (including configuration via the host processor) from voltage reaches valid range until it's fully operational shall be less than **50** ms. See Section 4.1 for typical configuration REF-CONF-A.

Requirement GEN-008:

The Ethernet Switch shall support the switch-dependent features of rapid spanning tree protocol (RSTP).

Requirement GEN-009:

The Ethernet Switch shall support IEEE 802.1X [2].

Requirement GEN-010:

The Ethernet Switch shall support pinning the address of an authenticated peer (IEEE 802.1X [2]) to its port.

Requirement GEN-011:

Specify the following performance characteristics of the implementation (buffer(s) for input and output) in the documentation of the Ethernet Switch:

- Maximum Frame Buffer Size (overall) [bytes]
- Maximum Frame Buffer Size depending on frame size in bytes [number of frames]. This could be a function or a table.
- Configuration options to distribute and limit the buffer size per port and CoS queue.

Requirement GEN-012:

The allocation of memory or length shall be limited for each queue. The limits shall be configurable individually.

Requirement GEN-013:

The Ethernet Switch shall support mirroring for each port. This includes mirroring frames from multiple ports to a single port with filtering depending on Port, SA/DA MAC Addresses and VLAN membership. This includes local and remote mirroring. It shall be possible for remote mirroring to change the VLAN-ID. At least 16 rules shall be supported, each being applicable to an arbitrary subset of the overall ports (e.g. by using a port bitmask).

Requirement GEN-014:

The Ethernet Switch shall support disabling/enabling incoming and outgoing traffic per port on MAC Layer independently of the link state of the physical layer.

Requirement GEN-015:

Specify the following performance characteristics of the implementation:

- MAC to MAC delay

Informational GEN-016:

The Ethernet Switch may support IEEE 802.1AE MACsec [3].

Informational GEN-017:

The Ethernet Switch may support jumbo frames.

Requirement GEN-018:

If the Ethernet Switch supports jumbo frames, it shall be possible to turn this off.

Requirement GEN-019:

The Ethernet Switch shall allow to uniquely identify the device and its revision (e.g. by a Device ID or similar). This shall be accessible via the configuration interface.

3.2 Address Resolution (ADDR)

This section describes requirements concerning the address resolution logic inside Ethernet Switches.

Requirement ADDR-001:

The Ethernet Switch shall support the learning of MAC addresses to the address table(s).

Requirement ADDR-002:

The address table shall be able to store **1024** MAC addresses simultaneously.

Requirement ADDR-003:

256 out of the total address table entries shall be stored without address conflict even if there is a conflict in the L2 address table. These can be learned or configured.

Requirement ADDR-004:

It shall be possible to read and write entries to the address table(s) by the host processor.

Requirement ADDR-005:

The Ethernet Switch shall support enabling/disabling of aging of address table entries for each entry individually.

Requirement ADDR-006:

The Ethernet Switch shall support adjusting the aging time of address table entries. This is only a single value for all learned entries.

Requirement ADDR-007:

It shall be possible to enable/disable the learning of MAC addresses to the address table(s) for each port individually.

Requirement ADDR-008:

The handling of frames with no match in the address table(s) for their destination address shall be configurable for each ingress port individually. It shall support:

- flooding the frame to all ports
- discarding the frame
- forward the frame to one port

Requirement ADDR-009:

Handling of MAAP addresses (91:E0:F0:00) and another user defined address range with no match in the address table(s) for their destination address shall be configurable. It shall support:

- flooding the frame to all ports
- discarding the frame
- forward the frame to one port

Requirement ADDR-010:

The handling of "01:80:C2" addresses shall be configurable. It shall support:

- flooding the frame to all ports
- discarding the frame
- forward the frame to one port

Requirement ADDR-011:

The Ethernet Switch shall provide a status information to indicate an overflow or a conflict in the address tables with the corresponding dropped MAC address.

Requirement ADDR-012:

The Ethernet Switch shall allow configuring that all incoming frames of selected switch ports are forwarded to a configured switch port (e.g. host controller).

Requirement ADDR-013:

The Ethernet Switch shall allow to configure address learning in a one-shot-mode.

Requirement ADDR-014:

The Ethernet Switch shall allow to limit the number of MAC Addresses learned on a port by a configuration parameter.

3.3 Virtual LANs (VLAN)

This section describes requirements concerning VLANs.

Requirement VLAN-001:

The Ethernet Switch shall support VLAN handling according to IEEE 802.1Q [4].

Requirement VLAN-002:

The Ethernet Switch shall support at least **1024** different VLAN-IDs which can be chosen freely from the entire range of all available 4096 VLAN-IDs.

Requirement VLAN-003:

It shall be possible to change/overwrite the VLAN-ID at the ingress port to a configured Default VLAN-ID. This includes untagged frames.

Requirement VLAN-004:

It shall be possible to perform Untagging depending on the VLAN-ID on any port upon egress.

Requirement VLAN-005:

The Ethernet Switch shall support Double-Tagging (Q-in-Q) according to IEEE 802.1Q [4].

Requirement VLAN-006:

The value for the outer TPID EtherType according to IEEE 802.1Q [4] shall be freely configurable.

Requirement VLAN-007:

The Ethernet Switch shall allow dropping of incoming packet that Double-Tagged (Q-in-Q) according to IEEE 802.1Q [4]. This feature has to be configurable for each port individually.

Requirement VLAN-008:

VLAN Re-Tagging shall be possible on egress based on the VLAN-ID. At least 16 rules shall be supported, each being applicable to an arbitrary subset of the overall ports (e.g. by using a port bitmask).

Requirement VLAN-009:

The Ethernet Switch shall suppress traffic with multiple 802.1Q customer tags (EtherType 0x8100) changing VLANs (VLAN hopping).

3.4 Quality of Service and Audio/Video Bridging (QOS)

This section presents requirements concerning Quality of Service and Audio/Video Bridging (AVB) features of Ethernet Switches.

Requirement QOS-001:

The Ethernet Switch shall support priority based quality of service according to IEEE 802.1Q [4].

Requirement QOS-002:

The Ethernet Switch shall support at least **8** different levels of priorities.

Requirement QOS-003:

The Ethernet Switch shall provide a queue for each priority on each egress port.

Requirement QOS-004:

The Ethernet Switch shall support strict priority scheduling for each egress port.

Requirement QOS-005:

The Ethernet Switch shall support at least one variant of Weighted Round Robin (WRR) or Weighted Fair Queuing (WFQ) scheduling for each egress port.

Informational QOS-006:

The Ethernet Switch may support more scheduling variants.

Requirement QOS-007:

The Ethernet Switch shall support mapping priority information based on 802.1Q priority bits depending on the incoming priority at the ingress port. This includes untagged frames (=Default priority).

Requirement QOS-008:

It shall be possible to overwrite the priority of a frame at an ingress port independent of the incoming priority (Global Priority Overwrite).

Requirement QOS-009:

Incoming priorities shall be freely mappable to internal queues.

Requirement QOS-010:

Frames of internal queues shall be freely mappable to priorities according to IEEE 802.1Q on egress.

Requirement QOS-011:

The Ethernet Switch shall support at least **8** shapers per egress port.

Requirement QOS-012:

The shapers shall support the leaky bucket algorithm. The algorithm used shall be configurable per shaper.

Requirement QOS-013:

The shapers shall support the credit-based shaper algorithm according to IEEE 802.1Q FQTSS [4]. The algorithm used shall be configurable per shaper.

Requirement QOS-014:

It shall be possible to deactivate each shaper individually.

Requirement QOS-015:

The Ethernet Switch shall fully support implementing the AVnu Automotive Profile including bridge and endpoint features in the ECU containing the Ethernet Switch [5].

3.5 Time Synchronization (TIME)

This section describes requirements concerning the time synchronization protocols.

Requirement TIME-001:

The Ethernet Switch shall support the PTP 1-step transparent clock according to IEEE 1588 [6].

Requirement TIME-002:

The Ethernet Switch shall support time synchronization on all ports.

Requirement TIME-003:

The Ethernet Switch shall support for non-standard MAC address, VLAN ID, and EtherType of PTP frames.

Note: This is needed for legacy implementations. For new implementations a better alternative based on the “sdold” is added to next version of 1588.

Requirement TIME-004:

The Ethernet Switch shall support running IEEE 802.1AS [7] and PTP 1-step transparent clock in parallel but on different ports.

Requirement TIME-005:

The Ethernet Switch shall support bridge and host implementations of IEEE 802.1AS [7].

3.6 Filtering of Incoming Frames (FILT)

This section describes requirements concerning the filtering of incoming Ethernet frames.

Requirement FILT-001:

The Ethernet Switch shall allow dropping incoming packets with VLAN-IDs according to IEEE 802.1Q [4] that are not configured for this port (membership check). This feature has to be configurable and shall cover untagged frames as well (default tag).

Requirement FILT-002:

The Ethernet Switch shall support a configurable bandwidth limitation (policing) for each ingress port based on priority or based on VLAN-ID.

Requirement FILT-003:

The Ethernet Switch shall support at least **8** policers per port.

Requirement FILT-004:

The Ethernet Switch shall support broadcast storm protection for each ingress port.

Requirement FILT-005:

The Ethernet Switch shall support unknown multicast storm protection for each ingress port.

Requirement FILT-006:

The Ethernet Switch shall provide status information that indicates if ingress filter policing occurred with the affected number of frames.

Requirement FILT-007:

The Ethernet Switch shall support filtering on L2 fields.

Requirement FILT-008:

The Ethernet Switch shall support filtering based on L3 and L4 addresses (i.e. IP Addresses and L4 Ports).

Requirement FILT-009:

The Ethernet Switch shall support filtering on ARP messages.

Requirement FILT-010:

The Ethernet Switch shall support filtering on IEEE1722 [14] frames.

Requirement FILT-011:

The Ethernet Switch shall support “forward” and “drop” as filtering actions per filtering rule (see requirements FILT-007, FILT-008, FILT-009, and FILT-010).

3.7 Diagnostics (DIAG)

This section describes requirements concerning diagnostics features of Ethernet Switches.

Requirement DIAG-001:

The Ethernet Switch shall provide at least the following counters individually for each port:

- number of received frames
- number of received bytes
- number of dropped frames after reception
- number of sent frames
- number of unsuccessful sent frames
- number of sent bytes
- maximum fill level of the queues since clearing the counter

Requirement DIAG-002:

The Ethernet Switch shall provide access to counter and status information of integrated PHYs.

Requirement DIAG-003:

Reading and resetting counter or status information in general shall be atomic.

Requirement DIAG-004:

The Ethernet Switch shall support cable diagnostics for each port with integrated PHYs.

Requirement DIAG-005:

Performance counters based on SNMP MIBs shall be supported.

Requirement DIAG-006:

The Ethernet Switch shall provide the following status information individually for each port on which an integrated Phy is used:

- link state

3.8 Interfaces (INTF)

This section describes requirements concerning external interfaces.

Requirement INTF-001:

100BASE-TX ports shall support Auto MDI-X.

Requirement INTF-002:

The Ethernet Switch shall support configuration over a SPI interface.

3.9 Configuration (CONF)

This section describes requirements concerning the configuration of Ethernet Switches.

Requirement CONF-001:

It shall be possible to change the configuration of the Ethernet Switch during runtime without disabling or blocking the Ethernet Switch (non-stop forwarding).

Requirement CONF-002:

All port-based features shall be configurable for each port individually.

Requirement CONF-003:

The Ethernet Switch shall support starting in "don't forward" mode before configuration is done.

Requirement CONF-004:

It shall be possible to read back all configuration information that can be written.

Requirement CONF-005:

The Ethernet Switch shall support selective lock down of configuration items until next cold start.

4 Typical Configurations

This section describes typical configuration sets in order to benchmark the configuration time of Ethernet Switches.

4.1 Reference Configuration A (REF-CONF-A)

The Reference Configuration A shall have at least the following elements:

- 12 VLANs
- 20 Multicast Addresses
- 8 priority queues
- 8 ingress policers per port
- 2 AVB queues with Shaper per port
- 1 regular Shaper per Port.
- Strict Priority scheduler.

5 References

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